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(21)Application number : 2000-306763 (71)Applicant : AGILENT TECHNOL INC

(22)Date of filing : 05.10.2000 (72)Inventor : BLEDSOE JAMES DAREN
CROFT DANIEL I
KELLY MICHAEL G

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(54) INTEGRATED CIRCUIT ASSEMBLY

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an integrated circuit assembly of chips formed of two or more non-interchangeable IC processes capable of reducing the

cost and hardly affected by the influences of an inductance and an EMI and suppressing its size.

SOLUTION: A daughter die 22 stacked on a mother die 14 is provided on the integrated circuit assembly, circuit layers 32, 50 of the dies are opposed to each other, and the dies are connected with a conductive layer or a solder bump.

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CLAIMS

[Claim(s)]

[Claim 1] Said DOTA die is an integrated-circuit assembly characterized by having an inferior surface of tongue containing two or more conductive contact pads to which alignment was carried out to each of said contact pad of said mother die, and each was connected electrically including the mother die which has a top face containing two or more conductive contact pads, and the DOTA die connected to said top face of said mother die.

[Claim 2] For the inferior surface of tongue of said DOTA die, said top face of said

mother die is the integrated-circuit assembly according to claim 1 with which it was made for said circuitry layer of said die to counter including two or more circuitry layers including two or more circuitry layers.

[Claim 3] The integrated-circuit assembly according to claim 1 or 2 which contains a conductive layer between said dies.

[Claim 4] Some at least are integrated-circuit assemblies of said contact pad according to claim 1 to 3 which are a solder bump.

[Claim 5] Said DOTA die is an integrated-circuit assembly according to claim 1 to 4 which has a circumference edge, separates from said edge in the amount of said contact pad from which some at least differ, and is arranged.

[Claim 6] For said DOTA die, said mother die is an integrated-circuit assembly according to claim 1 to 5 created according to a different process criterion.

[Claim 7] Said mother die is an integrated-circuit assembly according to claim 1 to 6 which has minimum line width smaller than said DOTA die.

[Claim 8] Said DOTA die is an integrated-circuit assembly according to claim 1 to 7 which has an electrical-potential-difference capacity higher than said mother die.

[Claim 9] Said mother die is an integrated-circuit assembly according to claim 1 to 8 which has the high-voltage line which connects one of said the contact pads to the external contact pad left and arranged from said DOTA die.

[Claim 10] The integrated-circuit assembly containing the 2nd DOTA die connected to said top face of said mother die according to claim 1 to 9.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to a multichip integrated-circuit assembly, if it generally describes in a detail further about an integrated-circuit assembly.

[0002]

[Description of the Prior Art] The integrated circuit chip which controls complicated actuation in a small package is used for an electronic instrument. A special order design is performed so that application specialization mold integrated-circuit (ASIC) equipment may offer a specific function. Since the manufacture process which narrows the line breadth and spacing of a circuit pattern and makes a small configuration possible was developed, it becomes reducible, and the magnitude and

costs (cost) of components are also reduced, or a given chip size came to be equipped with the size of an ASIC chip in many functions. However, the small configuration below a certain threshold is not suitable for the I/O (I/O) electrical potential difference of whenever [middle / in which an ASIC chip is needed by other electronic parts which perform an interface].

[0003] Furthermore, the chip created in a selection integrated-circuit manufacture process may lack the function of a certain fixed request. For example, the chip created so that the miniaturization of a digital data processing facility (for example, CMOS) might be optimized is unsuitable to the analog signal processing which is probably desired ideally, DRAM, FeRAM, or a FLASH function all over a single circuit. Even when the function which does not have compatibility on a chip is normally combinable, a compromise will be reached or more in one of the functions.

[0004] In order to offer current and two incompatibility IC processes or more, two or more chips are needed. An extender chain restricts a working speed, become easy to be influenced of an inductance and EMI, and the cost of manufacture and a component is made to increase, and though regrettable, size will also be made to increase, if between components is separated at the usual spacing. In order to realize the miniaturization of size, two or more chips have been included in a single package. For example, U.S. Pat. No. 5,777,345 is indicating the multi-chip integrated circuit package by which a die is attached in the top face of a bigger die. Wire bonding connects to the circumference pad of a support die, and the circumference bonding pad of an upper part die is combined with the perimeter pad of a lead frame. However, in order to usually hold down bonding length to within the limits, this approach lacks the flexibility in the size, number, and location of the upper part die relevant to a support die with arrangement of a pad. Furthermore, a line and a loop-formation wire become long, and make the effect of an inductance increase by wire bonding's becoming long and restricting arrangement of a pad. Moreover, the height of a bonding wire loop formation must be held into a protection package, and an appearance becomes high rather than it is needed. Moreover, the gap between the circuits on the upper part of each laminating die restricts the advantage of EMI, and the top face of an upper part die is not covered.

[0005]

[Problem(s) to be Solved by the Invention] In view of the above trouble, it is hard to be influenced of an inductance and EMI, cost can also be made low, and the integrated-circuit assembly by the chip created in two or more incompatibility IC processes that size can also be stopped, and its assembly approach are needed.

[0006]

[Means for Solving the Problem] This invention conquers a limit of the advanced technology by offering the DOTA die by which the laminating was carried out on the mother die to an integrated-circuit assembly. The top face of a mother die has many

correspondence conductivity contact pads to which alignment of the inferior surface of tongue of a DOTA die was carried out to each of the contact pad of a mother die, and each was connected electrically including many conductive contact pads. A pad can be arranged in the location of arbitration including the location distant from the periphery of a DOTA die. The circuitry layer of a die can counter mutually and a die can still be connected by a conductive layer or the solder bump.

[0007]

[Embodiment of the Invention] Drawing 1 shows the circuit assembly 10 containing a printed circuit board 12, and it has the inferior surface of tongue 16 connected to the top face 20 of a substrate, the 1st integrated circuit chip 14, i.e., mother die. It has the inferior surface of tongue 24 connected to the top face 26 of a mother die electrically and mechanically, the 2nd integrated circuit chip 22, i.e., DOTA die.

[0008] A mother die has the upper part circuit section 32 near the top face 26 containing two or more layers which have the metal earth plate 30 on the inferior surface of tongue, and have the functional circuit of a chip. The upper layer 34 contains the redistribution layer material 40 which includes the electrical installation between the metal bonding pad 36, a mother die circuit and a bonding pad, and other selected positions on top in a periphery on top. A bonding wire 42 connects each bonding pad 36 to each bonding pad 44 on a substrate.

[0009] The DOTA die 22 serves as the vertical contrary to the mother die, the earth plate 46 separated from the mother die, it is up suitable, and the circuit section 50 is suitable caudad toward the mother die. The redistribution layer 52 covers the circuit section and supplies the selection electrical connection between the selection field of the inferior surface of tongue of a DOTA die, and the circuit element in the circuit section 50.

[0010] As shown in drawing 2 , much contact locations 54 are arranged around the field of a DOTA die. In each of those locations, it connects electrically between dies. In the operation gestalt of illustration, this connection is made to at least one of the dies by the soldered joint section 56 formed in a front face from the solder bump printed in advance. This contact location can be arranged without constraint and includes a center and the mid-position with a circumference location in the array of arbitration substantially [the connecting location on a DOTA die front face]. In order to avoid a short circuit, except for preparing the minimum spacing between locations, all locations are permissible. By this, it becomes possible to fill up the whole front face with much connection if needed, and connection becomes possible [being given to the location where the circuit has been arranged the optimal on a DOTA (or mother) die]. By avoiding superfluous use of the leading-about line to the location, a die field is reduced and an EMI problem is also reduced.

[0011] In a suitable operation gestalt, a mother die and a DOTA die are created from various semiconductor chip creation process criteria, and each criterion is chosen so

that the priority matter of the engine performance of each chip, cost, and others may be optimized. In an example, a mother die is the high-speed CMOS chip which has the minimum size pattern configuration, and is used with a low-battery signal. A DOTA die is created according to a large-sized-like process criterion, and includes the drive circuit which changes a low-battery signal into the high line voltage needed by other circuits arranged to locations other than a substrate, or the exterior of a substrate. Therefore, the output signal generated on a mother die using the high-speed function is transmitted even to a DOTA die through one connection 56, and the circuit of a DOTA die increases the signal to the high voltage. This high-voltage signal is transmitted to a mother die through different connection. From there, it has "lockout" space suitable on a mother die, and a line broader than the minimum criterion carries the high-voltage signal to a bonding pad 36. It separates from this high-voltage line appropriately, and other circuits on a mother die can be arranged, in order to avoid the EMI effectiveness. Although a mother die can carry a simple high-voltage signal, it cannot process the signal of such an electrical potential difference.

[0012] It sets in a suitable operation gestalt, and the die is turned so that spacing other than the thickness of the min of the soldered joint section may counter that there is substantial completely nothing. This surface contiguity presses down electric conduction path length to the minimum, and reduces an inductance and the EMI effectiveness by it. Furthermore, "the Faraday cylinder (cage)" which reduces an EMI problem further is formed in the field of the outermost part of these sandwiches by having earth plates 30 and 46. Substantially, a part of all DOTA die circuits and mother die circuits are included between the earth plates of this cage. Moreover, since the highest field of this package, i.e., the earth plate of a DOTA die, does not include at all the circuit or connection which is easy to break, it is especially strong. Therefore, a strong assembly is offered even when there is not covering or an inclusion agent.

[0013] Moreover, the height of a required package will be lowered because there is no protrusion association, and this has many becoming [an important factor]-in small electronic instrument with which assembly is used cases. Since being based on the same silicon substrate member is desirable, a mother die and a DOTA die share a coefficient of thermal expansion, do not have the big stress in connection and are borne at the temperature of the broad range.

[0014] As shown in drawing 3 , two or more DOTA dies 22a and 22b can be installed on a single mother die. Size may differ from a function and those DOTA dies may be created from a further different process. It adjoins mutually and a DOTA die can be arranged, when a dimensional tolerance is precise, or when spacing is min so that it may illustrate, the alignment to a connecting location 54 is possible for it irrespective of all deformation in the edge dimension of the DOTA die relevant to a DOTA pattern. A DOTA die can be arranged like a suitable operation gestalt in all locations other than the field of a bonding pad, and the need gap for bondings. When a mother die is

connected without needing remarkable height or a remarkable gap, a DOTA die can be connected in all locations.

[0015] A DOTA die can be attached in a mother die by every optimal means for making connection between two front faces of a semiconductor chip. Drawing 4 shows a suitable operation gestalt and each of a mother die and a DOTA die has one solder bump 60 to each connection. It connects with the redistribution layer 40 on each die, and this solder bump supplies electrical installation to a desired circuit. Drawing 5 shows the deformation in which a DOTA die has the solder bump 60, and a mother die has the positioning metal contact 62 in a corresponding location. According to the surface tension effectiveness of the dissolved solder, self align of the DOTA die is carried out during a soldering process.

[0016] Drawing 6 shows the further alternative gestalt by which a metal or the redistribution layer contact pad 64 is supplied to each connecting location on both a DOTA die and a mother die. In a process without soldering, electroconductive glue has the anisotropy property for which current can only be conducted perpendicular, and prevents the short circuit during the adjoining connection. Such adhesives are known also as "Z-axis adhesives." The liquid or paste sprinkled over the whole front face is sufficient as these adhesives, or they may be alternatively applied to each pad. In that case, it becomes isotropy. Or the sheet or piece of solid-state electroconductive glue may be arranged between a mother and contact of DOTA for Z-axis electric conduction, and in that case, the adhesives act and are hardened by heat treatment.

[0017] The above is not suitable and the thing which meant that this invention was limited such, although explained in relation to the alternative implementation gestalt.

[0018]

[Effect of the Invention] As mentioned above, if this invention is used, in the integrated-circuit assembly of the chip created in two or more incompatibility IC processes, it is hard to be influenced of an inductance and EMI, and cost is also cheap and size can also be stopped.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view which met the line 1-1 of drawing 2 of the circuit assembly by the suitable operation gestalt of this invention.

[Drawing 2] It is the top view of the circuit assembly of drawing 1 .

[Drawing 3] It is the top view of the circuit assembly by the alternative implementation gestalt of this invention.

[Drawing 4] It is the decomposition sectional view of the alternative implementation gestalt of this invention.

[Drawing 5] It is the decomposition sectional view of the alternative implementation gestalt of this invention.

[Drawing 6] It is the decomposition sectional view of the alternative implementation gestalt of this invention.

[Description of Notations]

10: Integrated-circuit assembly

12: Printed circuit board

14: Mother die

16: The inferior surface of tongue of a mother die

20: The top face of a substrate

22a, 22b: DOTA die

24: The inferior surface of tongue of a DOTA die

26: The top face of a mother die

30: Metal earth plate

32: Up circuit section

34: The upper layer of a mother die

36: Bonding pad

40: The redistribution layer of a mother die

42: Bonding wire

44: Bonding pad

46: Earth plate

50: Circuit section

52: The redistribution layer of a DOTA die

54: Contact location

56: Soldered joint section

60: Solder bump

62: Metal contact

64: Contact pad